

UNITED STATES PATENT AND TRADEMARK OFFICE  
**CERTIFICATE OF CORRECTION**

PATENT NO. : 7,057,216 B2

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APPLICATION NO. : 10/698122

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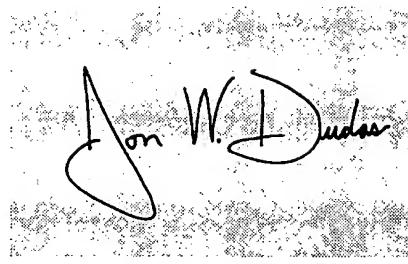
It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title page, item [57] Abstract: should read as follow:

A structure, and method of fabrication, for high performance field effect devices is disclosed. The MOS structures include a crystalline Si body of one conductivity type, a strained SiGe layer epitaxially grown on the Si body serving as a buried channel for holes, a Si layer epitaxially grown on the SiGe layer serving as a surface channel for electrons, and a source and a drain containing an epitaxially deposited, strained SiGe of opposing conductivity type than the Si body. The SiGe source/drain forms a heterojunction and a metallurgical junction with the Si body that coincide with each other with a tolerance of less than about 10nm, and preferably less than about 5nm. The heterostructure source/drain is instrumental in reducing short channel effects. These structures are especially advantageous for PMOS due to increased hole mobility in the compressively strained SiGe channel. Representative embodiments include CMOS structures on bulk and on SOI.

Signed and Sealed this

Tenth Day of April, 2007



JON W. DUDAS  
Director of the United States Patent and Trademark Office